1. A method of making a hybrid magnetoelectronic spin-based memory cell comprising the steps of:

forming an electron spin-based memory element situated on a silicon based substrate; said electron spin-based memory element including:

i) a first ferromagnetic layer with a changeable magnetization state;

ii) a second ferromagnetic layer with a non-changeable magnetization state;

iii) a base layer which is less than 1 micron in thickness and is situated between said first ferromagnetic layer and said second ferromagnetic layer, said base layer comprising a material having electron levels that are not significantly affected by an electron spin;

forming a memory cell selector coupled to said electron spin-based memory element, said memory cell selector including a semiconductor based transistor isolation element also situated on said silicon based substrate.

2. The method of claim 1, wherein said electron spin-based memory element is formed on top of said semiconductor based FET and separated by an insulation layer.

3. The method of claim 1, wherein an impedance of the electron spin-based memory element is on the order of 1 ohm.

4. The method of claim 1 wherein a spin transimpedance increases as said electron spin-based memory element is made smaller in size.

5. The method of claim 1 wherein a resistance of said base layer is the same or larger than a transimpedance of said electron spin-based memory element.

6. The method of claim 1, further including a step of forming a second semiconductor based transistor isolation element coupling said electron spin-based memory element to a bit reference line.

7. The method of claim 1 wherein the semiconductor based transistor isolation element is a field effect transistor (FET).

8. The method of claim 1 wherein the semiconductor based transistor isolation element is a bipolar junction transistor (BJT).

9. The method of claim 1, further including a step of forming a read line coupled to read data from said electron spin-based memory element, and a step of forming a separate write line coupled to write data to said electron spin-based memory element.

10. The method of claim 9, wherein said write line uses a single polarity current pulse.

11. The method of claim 1, wherein said write line is formed from two overlapping write lines.

12. The method of claim 11, wherein said electron spin-based memory element only changes state when a current pulse is present on both of said two overlapping write lines.

13. The method of claim 1, wherein said electron spin-based memory element is a spin transistor.

14. The method of claim 1, wherein said base layer is grounded.

15. The method of claim 1, wherein both a current pulse and a voltage pulse are used to read data stored by said electron spin-based memory element.

16. A method of forming a hybrid magnetoelectronic spin-based memory cell including the steps of:

forming an electron spin-based memory element situated on a silicon based substrate; said electron spin-based memory element including:

i) a first ferromagnetic layer with a first changeable magnetization state comprising permalloy and/or cobalt;

ii) a second ferromagnetic layer with a second non-changeable magnetization state also comprising permalloy and/or cobalt;

iii) a conductive paramagnetic base layer which is less than 1 micron in thickness and is situated between said first ferromagnetic layer and said second ferromagnetic layer, said base layer comprising a paramagnetic material capable of conducting a spin polarized current;

forming a memory cell selector coupled to said electron spin-based memory, said memory cell selector including a semiconductor based isolation element.

17. The method of claim 16, wherein said electron spin-based memory element is stacked on top of a second electron spin-based memory element.

18. The method of claim 16, wherein said electron spin-based memory element and said second electron spin-based memory element share said memory cell selector.

19. The method of claim 16, wherein said electron spin-based memory element is a three terminal, current biased device.

20. The method of claim 16, wherein said conductive paramagnetic base layer is adapted to create a nonequilibrium population of spin polarized electrons and an equivalent nonequilibrium magnetization M.

21. The method of claim 20, wherein said nonequilibrium magnetization M in said paramagnetic conductive paramagnetic base layer base generates an electric field at an interface with said first ferromagnetic layer.

22. The method of claim 16, wherein said spin polarized current has an amplitude that varies based on whether said first changeable magnetization state and said second non-changeable magnetization state are parallel or antiparallel.

23. A method of forming a hybrid magnetoelectronic spin-based memory cell including the steps of:

forming an electron spin-based memory element situated on a silicon based substrate, said electron spin-based memory element including:

i) a first ferromagnetic layer with a changeable magnetization state;

ii) a second ferromagnetic layer with a non-changeable magnetization state;

iii) a base layer which is less than 1 micron in thickness and is situated between said first ferromagnetic layer and said second ferromagnetic layer, said base layer comprising a conductive paramagnetic material capable of carrying a spin polarized current;

iv) a low transmission barrier also situated between said first ferromagnetic layer and said second ferromagnetic layer;

forming a semiconductor based isolation element coupled to said electron spin-based memory.

24. The method of claim 23, wherein said electron spin-based memory element is formed on top of said semiconductor based FET and separated by an insulation layer.

25. A method of forming a hybrid magnetoelectronic spin-based memory cell including the steps of:

forming an electron spin-based memory element situated on a silicon based substrate; said electron spin-based memory element including:

i) a first ferromagnetic layer with a changeable magnetization state comprising permalloy and/or cobalt;

ii) a second ferromagnetic layer with a non-changeable magnetization state also comprising permalloy and/or cobalt;

iii) a base layer which is less than 1 micron in thickness and is situated between said first ferromagnetic layer and said second ferromagnetic layer, said base layer being capable of carrying a spin polarized current;

iv) a low transmission barrier interface between said base layer and said first ferromagnetic layer, said low transmission barrier interface being configured to effectuate a unipolar voltage output for the hybrid magnetoelectronic spin-based memory cell;

forming a semiconductor based isolation element coupled to said electron spin-based memory element.

26. The method of claim 25, further wherein said low transmission barrier interface is configured to effectuate an impedance for the base layer which is larger than a transimpedance of said electron spin-based memory element.

27. The method of claim 25, further including a step of forming a second low transmission barrier interface associated with said second ferromagnetic layer.

28. The method of claim 25, wherein said base layer is a paramagnetic material in which an equilibrium energy level is substantially the same for two different electron spins.

29. The method of claim 25, further including a step of forming a read line coupled to read data from said electron spin-based memory element, and a forming a separate write line coupled to write data to said electron spin-based memory element.

30. A method of making a hybrid magnetoelectronic spin-based memory cell on a silicon based substrate comprising the steps of:

i) fabricating a semiconductor transistor in the silicon based substrate, which semiconductor transistor functions to isolate the hybrid magnetoelectronic spin-based memory cell from other devices in an array of hybrid magnetoelectronic spin-based memory cells;

ii) fabricating a first ferromagnetic layer with a first coercivity over the semiconductor transistor;

iii) fabricating an aluminum base layer on said first ferromagnetic layer;

iv) fabricating a second ferromagnetic layer with a second coercivity that is smaller than said first coercivity;

wherein step (ii) includes a step of introducing a low transmission barrier at an interface that is situated between said aluminum base layer and said second ferromagnetic layer;

wherein an impedance of the hybrid magnetoelectronic spin-based memory cell to a spin polarized current can be varied to store data.

31. The method of claim 30, further including a step: forming said semiconductor transistor as an enhancement mode field effect transistor.

32. The method of claim 30, further including a step of forming a write line over said second ferromagnetic layer.

33. The method of claim 32, further including a step of forming a read line separate from said write line.

34. The method of claim 30 further including a step of forming a plurality of additional hybrid magnetoelectronic spin-based memory cells in separate layers in a stack arrangement over said semiconductor transistor.

35. The method of claim 33 wherein said semiconductor transistor also functions to isolate all of the plurality of additional hybrid magnetoelectronic spin-based memory cells.

36. The method of claim 30, further including a step of forming a second low transmission barrier interface associated with said second ferromagnetic layer.

37. The method of claim 30, wherein said aluminum base layer is adapted to create a nonequilibrium population of spin polarized electrons and an equivalent nonequilibrium magnetization M.

38. The method of claim 37, wherein said nonequilibrium magnetization M in said aluminum base layer base generates an electric field at an interface with said first ferromagnetic layer.

39. The method of claim 30, wherein said spin polarized current has an amplitude that varies based on whether a first changeable magnetization state of said first ferromagnetic layer and a second non-changeable magnetization state of said second ferromagnetic layer are parallel or antiparallel.